Abstract

Ultra-low power (ULP) MOS diode

The present invention relates to an ultra-low power (ULP) MOS diode. The diode has a first and a second terminal. It comprises an n-MOS transistor having a channel, a first N+ doped diffusion region at one extremity of the channel and a second N+ diffusion region at the other extremity of the channel, and a p-MOS transistor having a channel and a first P+ doped diffusion region at one extremity of the channel and a second P+ diffusion region at the other extremity of the channel. The first N+ diffusion region of the n-MOS transistor is coupled to the first P+ diffusion region of the p-MOS transistor, the gate of the n-MOS transistor is coupled to the second P+ diffusion region of the p-MOS transistor, and the gate of the p-MOS transistor is coupled to the second N+ diffusion region of the n-MOS transistor. The second P+ diffusion region of the p-MOS transistor is coupled to the first terminal of the diode and the second N+ diffusion region of the n-MOS transistor is coupled to the second terminal of the diode. The diode has a current versus voltage characteristic such that it has a negative slope in a reverse biased state of the diode.

Abstract

Cancel the previous abstract submitted with the application and substitute that attached.